High Frame Frequency CMOS Imaging System Based on FPGA

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Abstract: Based on the GMV300 sensor of CMOSIS company, a high resolution imaging system is designed in this paper. This paper introduces the main characteristics of CMV300 detector chip, and realizes the driving of detector control signal and the receiving of high-speed LVDS transfer line image data by using FPGA. The hardware and software modules of the prime minister system are designed by the operating parameters on the SPI bus configuration sensor. Finally, the CMOS camera imaging system is simulated and tested. The results show that the system can satisfy the requirement of time sequence and output stable images.

1. Introduction

The image sensor is the core of photo electronic imaging equipment. The main advantage of a CCD image sensor and CMOS two.CCD detector of high sensitivity, low noise, the disadvantage is driven and complex, processing circuit power consumption; the main advantages of the CMOS detector is high integration, low power consumption, simple peripheral circuit, the disadvantage is large dark current. Image noise and sensitivity than CCD. but after years of improvement process, now the CMOS sensor can reach CCD sensor image quality at the same time can provide much higher than the CCD sensor frame rate and data output rate. Therefore, the selection of design .The imaging system is designed with the CMV300 image sensor of CMOSIS company. The XQR4VSX55-10CF1140V FPGA chip in the V4 series of Xilinx company is used as the main processor.

2. System Structure

The functional block diagram of the imaging system is shown in Figure 1. Includes optical systems， CMV300 image sensor imaging and image processing parts, interface part and power part.

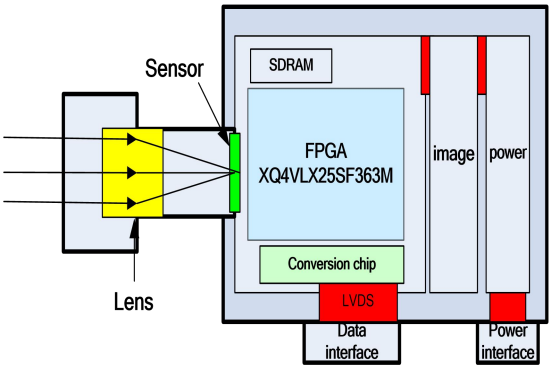

Figure 1: Overall design block diagram.

Imaging and image processing part of the image sensor needs to produce a variety of working time sequence of optical image into digital electricity and image signal, and according to the specified sequence read out and image sensor output signal acquisition, conversion to standard video stream. Color reduction into color video signal to achieve automatic exposure automatic gain automatic white balance function. In the interface part, the video stream processed by Beijing FPGA is converted into the required format for output, and communication with other systems is realized according to the overall requirements. The power supply part converts the current supplied into the various secondary currents required inside the HD camera.

3. Detailed Design

3.1. CMV300 Image Sensor

Image sensor is the core of imaging equipment, and the selection of sensor relates to the whole system performance. In order to meet the technical requirements of high-speed video camera, we use 648×488 CMOS imaging detector of CMOSIS company to realize high-performance imaging under high-resolution and low-illumination haze.

Figure 2 shows the CMV300 image sensor outline and the bright sub sales curve. CMV300 image sensor is produced by massaging company who produces a large-area town CMOSIS image sensor and effective number of pixels is 640×480, Pixel size is 7.4μm×7.4μm, Dynamic range up to 60 dB .The highest treasures of the detector are 180fps, Only 16 high-speed train trip with LVDS interface output image data, data transmission frequency of up to 480Mbps, data accuracy of up to 10bit. CMV 300 with global electronic shutter function can be based on the actual work needs, accurate control of exposure time to ensure the quality of imaging system.

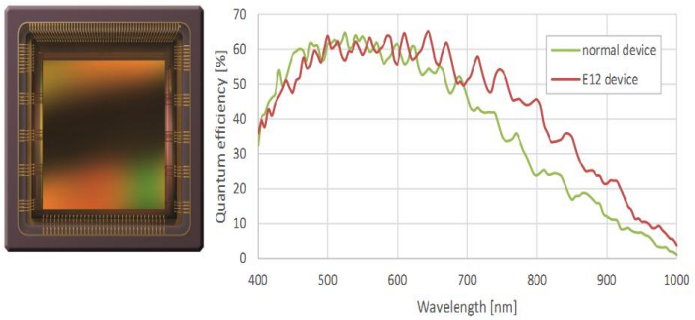

Figure 2: Schematic diagram of shape and quantum efficiency distribution of CMV300 CMOS device.

3.2. Power Supply Design

The normal operation of the CMV300 requires three supply voltages,+3.3V, +3.0V and +2.0V respectively . The supply voltages required for FPGA are +3.3 V, +2.5 V and +1.2V. Imaging system, using 5 V voltage input, considering the system voltage type and current demand, decided to use LINEAR company LT1764 chip to complete the +5V to +3.3V,+3V,+2V,+2.5V and +1.2V voltage conversion. Figure 3 is a typical circuit of LT1764.The SHDN is an odd switching control signal, and the output voltage can be switched by changing the level of the signal according to the demand. In order to ensure the detector works stably and normally, power supply management is needed. After the whole system is electrified, FPGA realizes the sequence electrification of the three kinds of power supplies by controlling the level of l/O.In Figure 3, the output voltage of l t can be changed by adjusting the resistance values of R 1 and R 2, as shown in the calculation 1.

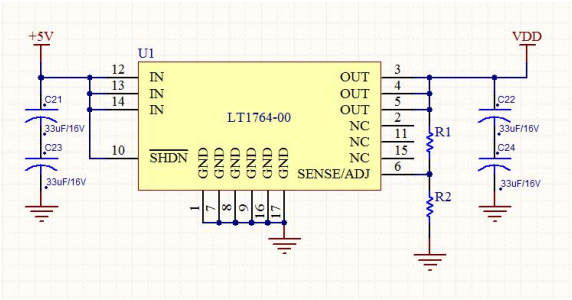

Figure 3: Schematic diagram of power supply voltage conversion.

3.3. Main Functions of FPGA

After selecting the C MOS image sensor, the peripheral circuit should be designed to provide the driving signal and register configuration for the main controller, and then the main controller should receive the video signal. And according to the characteristics of the implementation of the video signal processing, conversion to meet the requirements of the video stream. The main functional circuit diagram of FPGA is shown in Figure 4. The function of image sensor timing control and image processing is realized in

FPGA. This part is mainly to CCMOS, SDRAM driver, get image data. The processing of image data includes the functions of automatic exposure, automatic gain-adding and data package sending.

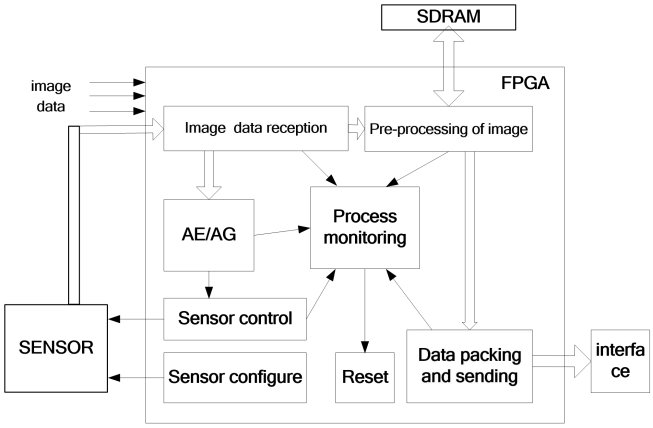

Figure 4: FPGA functional block diagram.

Power system, FPGA requires a program load (load T < = 2S).FPGA reset signal (T<= 100ms), for SDRAM, CMOS, and FPGA. The internal program reset reset after the completion of the first CMOS, the state of the sensor configuration.SPI interface configuration is completed, the camera into the normal working state of the SPI interface configuration simulation timing diagram is shown in Figure 5.

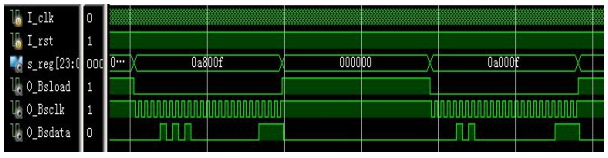

Figure 5: Simulation sequence Diagram of SPI Interface configuration.

Under normal working condition, the image sensor control module implements the exposure time and frame rate according to the time specified by CMOS. The external exposure mode of. CMOS is shown in Figure 6 as shown in Figure 6.

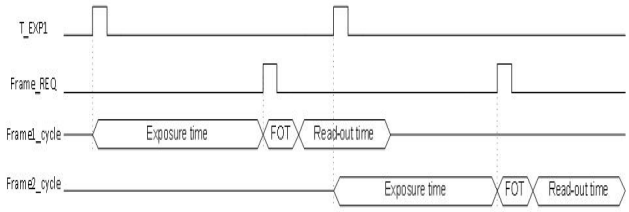

Figure 6: How CMOS external exposure works.

CMOS output image data according to the control signal. After receiving the image data module, the image data flow format is formed. Image data flow format is shown in Figure 7.

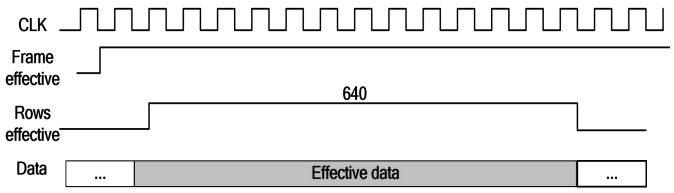

Figure 7: Image data flow format.

The image data is reserved for two routes, one for automatic exposure and one for automatic gain module. The calculated results are fed back to the image sensor control module for controlling exposure time. Another image data stream provides image pre-processing module for image precision conversion gain control and other real-time image pre-processing module.

Image data after image pre-processing. The packaged send module sends data in the specified format to other devices.Data output format, as shown in Figure 8. A total of 640 rows of image data, each line of 480 .The rising edge of the clock data effectively. Frame valid signal is high and the effective signal transmission line is high, said image. Effective signal lasts 2560 CLK. data channel 1Byte data of each pixel to low in serial data before (D0, D1, D2, D3, D4, D5, D6, D7) the output data transmission channel 1. Each line of the image data of the lower four (D0, D1, D2, D3), each data channel 2 image data of the high four bits (D4, D5, D6, D7).

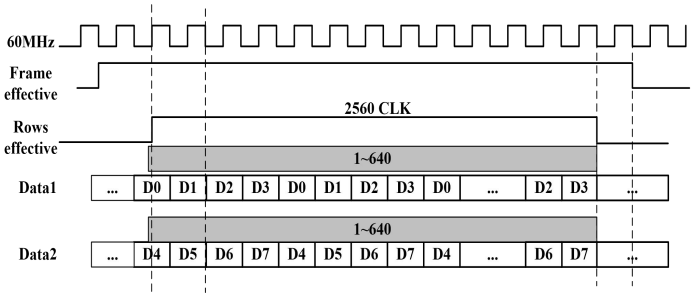

Figure 8: Data output format.

3.4. Interface Board Design

The function of the interface board is to receive and send LVDS signals. The chip is DS90LV031A, DS90LV032A, and the chip's working voltage is 3.3V, encapsulated as W16A. The quality level is military level. The static power consumption is only 330 μW. The driving and receiving wave forms of the DS90LV031A are shown in Figure 9, respectively.

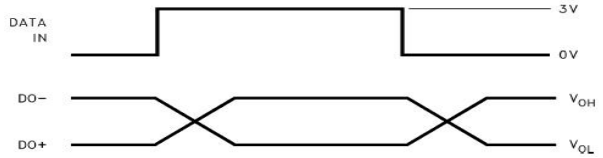

Figure 9: Typical driving output Waveform of DS90LV031A.

The output data signal interface defines a connection as shown in Figure 10: the LVDS transmitter, the logic "1" to two line voltage difference between +350mV; logic "0" to two line voltage difference between -350mV. LVDS synchronization transmission interface as a communication interface of image transmission controlled by a data valid signal and a serial clock. The time interval of data acquisition of effective signal effectively, a serial digital signal sent by the camera. Each byte is transmitted first MSB (MSB) until the lowest (LSB). Data and effective signal by the rising edge of the clock control. The clock signal is always transmitted. When the effective data is sent, the effective signal is low logic "0" or the logic high "1".

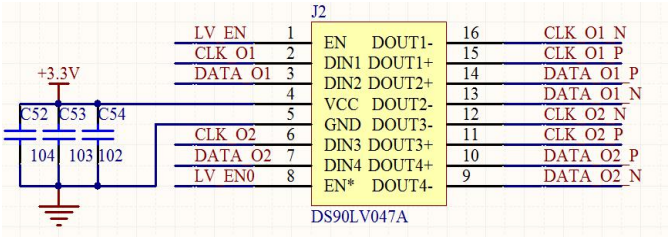

Figure 10: LVDS data interface diagram.

4. Experimental Results and Analysis

According to the above principle, the design of CMOS imaging system based on FPGA is completed. The imaging experiment is carried out to verify the actual performance of the system and to test the actual imaging performance of the whole CMOS imaging system. After the completion of circuit debugging, the structure of the machine is adjusted.

After the optical lens is installed, the actual image is made for the external scene. The captured image is shown in Figure 11. It can be seen that the imaging effect of the detector with the lens is good, and it can make a clear imaging of the actual scene.

Figure 11: An image taken by an imaging system.

5. Conclusions

However, FPGA is the main control chip in the video acquisition system. First, the CMOS image sensor is selected, and then the key components are analyzed, and the control technology is designed to realize

the data acquisition of the output video signal of Cmv300 digital image sensor. Data processing, data caching and video final display. The results show that the system is a kind of CMOS image sensor acquisition system with excellent performance and high stability. It has a very wide range of applications.

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